SIMULTANEOUS BIDIRECTIONAL INPUT/OUTPUT CIRCUIT AND METHOD

BACKGROUND OF THE INVENTION

Related Applications

This application claims the benefit of Korean Patent Applications No. 2002-87887, filed December 31, 2002 and 2003-25085, filed April 21, 2003, the disclosures of which are hereby incorporated herein by reference.

1. Field of the Invention

The present invention relates to semiconductor devices employing simultaneous bi-directional (SBD) transmission, and more particularly to methods and apparatus for SBD input/output circuits for such devices.

2. Description of the Related Art

Semiconductor devices such as processors, controllers, memory devices, etc., are commonly equipped with data transceivers that allow them to receive and transmit digital signals. Conventionally, such transceivers are reconfigurable to either receive or transmit data across an attached transmission line. Recently, devices with *simultaneous bi-directional* (SBD) transmit/receive capability have received increased interest. As the name alludes to, SBD transceivers have the capability to receive and transmit digital data during the same clock cycle, on the same transmission line.

Figure 1 shows a conventional SBD connection between two semiconductor devices 20 and 40. Devices 20 and 40 contain, respectively, SBD transceivers 22 and 42. SBD transceiver 22 contains a data driver 24 and a data receiver 26. An internal data signal to be driven, Dout1, is supplied as an input to driver 24 and as a control signal to receiver 26. The output of driver 24 is coupled to the input of receiver 26. Receiver 26 also receives two

reference voltages, *VrefH* and *VrefL*, which it uses for comparisons, as will be explained shortly. The output of receiver 26 is a data input, Din1, to device 20.

Transceiver 42 of device 40 is preferably matched to transceiver 22 of device 20. Transceiver 42 contains a driver 44 and a receiver 46 connected in an identical configuration as the driver and receiver of transceiver 22. Driver 44 takes its input from an internal data signal Dout2, and receiver 46 generates a data input Din2.

Semiconductor devices 20 and 40 can be connected to each other in the configuration shown in Figure 1, by connecting the outputs of drivers 24 and 44 to a transmission line 30. Note that in this configuration, the drive state of both driver 24 and driver 44 determine the voltage V_{BL} on transmission line 30. A common reference voltage generator 32 supplies *VrefH* and *VrefL* to both circuits.

Figure 2 contains waveforms illustrating the simultaneous exchange of data between devices 20 and 40 over transmission line 30. Dout1 is high during time periods T1, T2, and T5. Dout2 is high during time periods T1, T3, and T5. Consequently, during T1, drivers 24 and 44 both pull the voltage V_{BL} on the transmission line high, e.g., to an upper rail voltage V_h. During T2, driver 24 attempts to pull the voltage V_{BL} high and driver 44 attempts to pull V_{BL} low, e.g., to a lower rail voltage V_l. With matched drivers, V_{BL} will assume an approximate voltage V_{mid}, halfway between upper rail voltage V_h and the lower rail voltage V_l. During T3, both drivers reverse, and V_{BL} stays at V_{mid}. During T4, both drivers pull V_{BL} low, to V_l.

Receivers 26 and 46 determine the drive state of the other device's driver during each time period by selecting an appropriate comparison voltage, based on the known drive state of their own driver. For instance, during T1 and T2, receiver 26 knows that driver 24 is driving line 30 high—thus the only two possible values of V_{BL} are V_h (when driver 44 is also driving line 30 high) and V_{mid} (when driver 44 is driving line 30 low). Thus during T1,

receiver 26 selects the reference voltage *VrefH* in response to a logic high level on Dout1 and then compares V_{BL}, with its high level (Vh), to *VrefH*, at a level of 3/4 VDD, and outputs Din1 as a high level. Also, during T2, the receiver 26 also selects the reference voltage *VrefH* in response to a logic high level on Dout1 and then compares *VBL*, now with a V_{mid} level, to *VrefH*, at a level of 3/4VDD, and outputs Din1 as a low level. During T3, the receiver 26 selects the reference voltage *VrefL* in response to a logic low level on Dout1 and then compares *VBL*, with its V_{mid} level, to *VrefL*, at a level of 1/4 VDD, and outputs Din1 as a high level. Also, during T4, the receiver 26 also selects the reference voltage *VrefL* of 1/4 VDD in response to a logic low level on Dout1 and then compares *VBL*, now with a low level, to *VrefL*, at a level of 1/4 VDD, and outputs Din1 as a low level. Receiver 46 operates similarly, but based on the known state of driver 44, to determine the drive state of driver 24.

In some prior art implementations, the reference signals *VrefH* and *VrefL* are generated separately on each device. Some receivers use multiplexers, with Dout as a select signal, to decide which of the two reference signals will be compared to V_{BL}. Other receivers use a buffer to selectively generate one of *VrefH* and *VrefL* for comparison with V_{BL}.

In the prior art devices, the SBD receivers compare the voltage V_{BL} to a single reference voltage *VrefL* or *VrefH*, representing $0.25V_{DD}$ and $0.75V_{DD}$, depending on the value of Dout for that SBD device. Referring to Figure 3A, receiver 26 of Figure 1 compares V_{BL} to $0.75V_{DD}$ during time periods T1, T2, and T5, and compares V_{BL} to $0.25V_{DD}$ during time periods T3 and T4. Likewise and as shown in Figure 3B, receiver 46 compares V_{BL} to $0.75V_{DD}$ during time periods T1, T3, and T5, and compares V_{BL} to $0.25V_{DD}$ during time periods T2 and T4. Consequently, at each time period the maximum differential voltage applied to each differential receiver is approximately $0.25V_{DD}$. This small margin can be readily eroded by noise and driver mismatches, and can also be substantially affected by

small errors in the reference voltages *VrefL* or *VrefH*, which are not voltages naturally produced by SBD circuits during signaling.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates two prior-art SBD transceivers, on separate semiconductor devices, connected by a transmission line;

Figure 2 illustrates data input value/output value relationships for the transceivers of Figure 1;

Figures 3A and 3B show, respectively, the comparisons made by the two SBD transceivers of Figure 1 for various driven data states;

Figure 4 illustrates two SBD transceivers according to some embodiments of the present invention, connected by a transmission line;

Figures 5A and 5B depict, respectively, the comparisons made by the two SBD transceivers of Figure 4 for various driven data states;

Figure 6 illustrates two SBD transceivers according to other embodiments of the present invention, connected by a transmission line;

Figures 7A and 7B depict, respectively, the comparisons made by the two SBD transceivers of Figure 6 for various driven data states;

Figures 8 and 9 illustrate, respectively, a receiver circuit and reference selector useful in some embodiments of the present invention;

Figure 10 shows an alternate embodiment of a reference selector;

Figure 11 shows an alternate embodiment of a receiver circuit; and

Figure 12 illustrates a driver circuit useful in at least some embodiments of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The embodiments described herein seek to replace the single comparison between a voltage on the transmission line and a synthesized $0.25V_{DD}$ or $0.75V_{DD}$ reference voltage, as practiced in prior art SBD receivers. Succinctly stated, various receiver embodiments described herein use two comparison voltages that each approximate one of the two voltages that could appear on an SBD transmission line.

Figure 4 illustrates a configuration 50 comprising two semiconductor devices 60 and 70 connected by two transmission lines 80 and 90. Device 60 comprises an SBD input/output (I/O) circuit 100, and device 70 comprises an SBD input/output circuit 200. Transmission line 80 connects to an I/O pad 120 of SBD I/O circuit 100 at one end, and to an I/O pad 220 of SBD I/O circuit 200 at the other end. Transmission line 90 connects to a VREFM generator 190 on device 60 in order to supply VREFM to device 70 (alternately, each device can generate its own VREFM reference or the VREFM generator can only be located in the device 70). VREFM generator 190 can also supply VREFM to other SBD I/O circuits (not shown) on either device.

SBD I/O circuit 100 comprises a driver 110, a reference selector 130, and a receiver 150. Driver 110 can operate in a conventional manner to drive an output signal Dout1 through pad 120 onto transmission line 80. Reference selector 130 uses output signal Dout1 to select a first reference voltage VREFD1 for input to receiver 150; VREFM generator 190 supplies a second reference voltage VREFM to receiver 150. A third input to receiver 150 connects to I/O pad 120, and therefore supplies a voltage V_{BL} to receiver 150. As will be explained shortly, receiver 150 uses VREFD1, VREFM, and V_{BL} from transmission line 80 to output a signal Din1 representative of the signal Dout2 signaled by SBD I/O circuit 200.

SBD I/O circuit 200 comprises a driver 210, a reference selector 230, and a receiver 250, configured substantially similarly to the corresponding elements of SBD I/O circuit 100.

The operation of receiver 150 will now be explained with reference to Figure 5A, with an underlying assumption that drivers 110 and 210 are capable of driving transmission line 80 to three possible voltages V_{DD}, V_{SS}, and $0.5(V_{DD} - V_{SS})$. To simplify the discussion, $V_{SS} = 0$ V will be assumed, although those skilled in the art recognize that other values of V_{SS} can be selected in a particular implementation, and voltages V_{DD} and V_{SS} may not represent full rail voltages in other implementations due to driver limitations.

During time periods T1 and T2, Dout1 is a logic high value, and therefore the two possible expected values of V_{BL} are V_{DD} and $V_{DD}/2$. VREFM generator 190 sets VREFM to $V_{DD}/2$, and reference selector 130 sets VREFD1 to V_{DD}, because the level of Dout1 is a high level. In other words, if the level of Dout1 is a low level, the reference selector 130 sets VREFD1 to V_{SS}. The reference selector 230 operates the same as reference selector 130. Receiver 150 thus compares V_{BL} to V_{DD} and $V_{DD}/2$, setting Din1 to a logic high value when V_{BL} is closer to V_{DD} (time period T1) and setting Din1 to a logic low value when V_{BL} is closer to $V_{DD}/2$ (time period T2).

During time periods T3 and T4, Dout1 is a logic low value, and therefore the two possible expected values of V_{BL} are $V_{DD}/2$ and V_{SS}. Accordingly, reference selector 130 sets VREFD1 to V_{SS}. Receiver 150 thus compares V_{BL} to $V_{DD}/2$ and V_{SS}, setting Din1 to a logic high value when V_{BL} is closer to $V_{DD}/2$ (time period T3) and setting Din1 to a logic low value when V_{BL} is closer to V_{SS}.

Figure 5B illustrates the similar operation of SBD I/O circuit 200 for the same Dout1/Dout2 drive sequence.

Figure 6 illustrates a configuration 55 comprising two semiconductor devices 65 and 75 connected by three transmission lines 85, 95 and 97. Device 65 comprises an SBD input/output (I/O) circuit 300, a VREFM1-1 generator 380, and a VREFM2-1 generator 390. Device 75 comprises an SBD input/output circuit 400, a VREFM1-2 generator 480, and a

VREFM2-2 generator 490. Transmission line 85 connects to an I/O pad 320 of SBD I/O circuit 300 at one end, and to an I/O pad 420 of SBD I/O circuit 400 at the other end. Transmission line 95 connects VREFM1-1 generator 380 on device 65 to VREFM2-2 generator 490 on device 75. Transmission line 97 connects VREFM2-1 generator 390 on device 65 to VREFM1-2 generator 480 on device 75.

SBD I/O circuit 300 comprises a driver 310 and a receiver 350 that functionally incorporates an internal reference selector. Driver 310 can operate in a conventional manner to drive an output signal Dout1 through pad 320 onto transmission line 85. Receiver 350 receives output signal Dout1, which it uses to operate a corresponding portion of the receiver. Five comparison voltages are supplied to receiver 350: rail voltages V_{DD} and V_{SS}, voltage V_{BL}, and voltages VREFM1-1 and VREFM2-1 generated respectively by reference generators 380 and 390. As will be explained shortly, receiver 350 uses these voltages to output a signal Din1 representative of the signal Dout2 signaled by SBD I/O circuit 400.

SBD I/O circuit 400 comprises a driver 410 and a receiver 450 configured substantially similarly to the corresponding elements of SBD I/O circuit 300.

The use of two mid-point reference voltages VREFM1 and VREFM2 on each device accounts for the possibility that drivers 310 and 410 may not be perfectly matched. In such a circumstance, slightly different voltages V_{BL} are observed when driver 310 attempts to pull the line high and driver 410 attempts to pull the line low, compared to when driver 310 attempts to pull the line low and driver 410 attempts to pull the line high (see Figure 7A, voltages V_{MID1} and V_{MID2} for V_{BL} during time periods T2 and T3, respectively). To increase the accuracy of the receiver operation, two different midpoint voltages are calculated and used in these two situations.

Generator 380 is matched to driver 310—or at least to the pull-up portion of driver 310—and has an input tied permanently to V_{DD} (or possibly a logic high signal) in one

embodiment. In operation, then, generator 380 is always attempting to pull line 95 high with the same strength that driver 310 attempts to pull line 85 high when Dout1 is a logic high value.

Generator 490 is matched to driver 410—or at least to the pull-down portion of driver 410—and has an input tied permanently to V_{SS} (or possibly to a logic low signal) in one embodiment. In operation, then, generator 490 is always attempting to pull line 95 low with the same strength that driver 410 attempts to pull line 85 low when Dout2 is a logic low value.

When generators 380 and 490 are connected by transmission line 95, a VREFM1-1 value is supplied to receiver 350 that should accurately match V_{BL} when Dout1 is a logic high value and Dout2 is a logic low value, even if drivers 310 and 410 are not perfectly matched. The same value is supplied to receiver 450 as VREFM2-2.

Generators 390 and 480 are constructed similar to their respective counterparts 490 and 380 and are connected in operation by transmission line 97. Accordingly, a VREFM2-1 value is supplied to receiver 350 that should accurately match V_{BL} when Dout1 is a logic low value and Dout2 is a logic high value, even if drivers 310 and 410 are not perfectly matched. The same value is supplied to receiver 450 as VREFM1-2.

The operation of receivers 350 and 450 can be better understood with reference to Figures 7A and 7B. Referring first to Figure 7A, during time periods T1 and T2, Dout1 is a logic high value, and therefore the two possible expected values of V_{BL} are V_{DD} and V_{MID1}. Accordingly, receiver 350 activates a portion of its circuitry that compares V_{BL} to V_{DD} and VREFM1-1, setting Din1 to a logic high value when V_{BL} is closer to V_{DD} (time period T1) and setting Din1 to a logic low value when V_{BL} is closer to V_{MID1} (time period T2).

During time periods T3 and T4, Dout1 is a logic low value, and therefore the two possible expected values of V_{BL} are V_{MID2} and V_{SS}. Accordingly, receiver 350 activates a

portion of its circuitry that compares V_{BL} to V_{MID2} and V_{SS}, setting Din1 to a logic high value when V_{BL} is closer to V_{MID2} (time period T3) and setting Din1 to a logic low value when V_{BL} is closer to V_{SS}.

Figure 7B shows a similar selection of comparison voltages for receiver 450. Because driver 410 drives opposite of driver 310 when V_{BL} is equal to V_{MID1} or V_{MID2}, however, the voltage values supplied to receiver 450 as VREFM1-2 and VREFM2-2 are switched from the corresponding values in Figure 7A.

Figure 8A contains a circuit diagram for some embodiments of a receiver 150 (or 250) as shown in Figure 4. The receiver comprises two differential amplifiers 151 and 153 and a load circuit 155.

Load circuit 155 comprises first and second matched load resistors R_L. One end of each resistor is connected to V_{DD}. The other end of the first resistor connects to a differential output node OUT; the other end of the second resistor connects to a second differential output node OUTB. An output stage (not shown) converts the voltage difference appearing across OUT and OUTB to a logic signal Din.

Differential amplifier 151 contains two matched depletion-mode N-channel MOSFET transistors N1 and N2, and a third N-channel MOSFET transistor N3. Transistor N3 has a drain connected to a tail current node, a source connected to V_{SS}, and a gate connected to an input node BIAS. BIAS is set by a biasing circuit (not shown) that sets the tail current I_A flowing from the tail current node through transistor N3, such that N3 acts as a current source for differential amplifier 151.

The sources of matched transistors N1 and N2 connect to the tail current node and therefore split tail current I_A according to the differential voltage applied to their gates. The gate of transistor N1 receives the signal VREFM from VREFM generator 190 (Figure 4), and

the gate of transistor N2 receives the voltage signal V_{BL}. The drain of N1 connects to output node OUT, and the drain of N2 connects to output node OUTB.

Differential amplifier 153 is identical to differential amplifier 151. Differential amplifier 153 contains two matched depletion-mode N-channel MOSFET transistors N4 and N5, and a third N-channel MOSFET transistor N6. Transistor N6 has a drain connected to a tail current node, a source connected to V_{SS}, and a gate connected to the input node BIAS. BIAS sets the tail current I_B flowing from the tail current node through transistor N6, such that N6 acts as a current source for differential amplifier 153 and $I_A = I_B$.

The sources of matched transistors N4 and N5 connect to the tail current node and therefore split tail current I_B according to the differential voltage applied to their gates. The gate of transistor N4 receives the voltage signal V_{BL}, and the gate of transistor N5 receives the signal VREFD1 from reference selector 130 (Figure 4). The drain of N5 connects to output node OUT, and the drain of N4 connects to output node OUTB.

Because differential amplifiers 151 and 153 both connect to load circuit 155, both tail current I_A and tail current I_B must flow from positive voltage rail V_{DD} through load circuit 155. The combined current $I_A + I_B$ is split between the two load resistors depending on the values of VREFM, VREFD1, and V_{BL}. For example, consider the conditions shown during time period T1 in Figure 5A, wherein V_{BL} = VREFD1 = V_{DD} and VREFM = $V_{DD}/2$. Under these conditions N2 will be driven harder than N1 and carry more than half of I_A, thus dropping the voltage at OUTB as compared to OUT. N4 and N5 will be driven approximately the same and will split I_B equally, and thus no differential voltage will appear across OUT/OUTB as a result of amplifier 153. The net effect is a positive differential voltage between OUT and OUTB, indicating that Din should be set to a logic high condition.

For time period T2 of Figure 5A, VREFD1 remains at V_{DD} and VREFM remains at $V_{DD}/2$, but V_{BL} drops to $V_{DD}/2$. Accordingly, N1 and N2 will be driven approximately the

same and will split I_A equally, and thus no differential voltage will appear across OUT/OUTB as a result of amplifier 151. N5 will be driven harder than N4, however, and carry more than half of I_B, thus dropping the voltage at OUT as compared to OUTB. The net effect is a negative differential voltage between OUT and OUTB, indicating that Din should be set to a logic low condition.

Continuing with time period T3 of Figure 5A, V_{BL} = VREFM = $V_{DD}/2$, but reference selector 130 now sets VREFD1 to V_{SS}. Accordingly, N1 and N2 will be driven approximately the same and will split I_A equally, and thus no differential voltage will appear across OUT/OUTB as a result of amplifier 151. N4 will be driven harder than N5, however, and carry more than half of I_B, thus dropping the voltage at OUTB as compared to OUT. The net effect is a positive differential voltage between OUT and OUTB, indicating that Din should be set to a logic high condition.

Finally, consider time period T4 of Figure 5A, when VREFD1 remains at V_{SS} and VREFM remains at $V_{DD}/2$, but V_{BL} drops to V_{SS}. Under these conditions N1 will be driven harder than N2 and carry more than half of I_A, thus dropping the voltage at OUT as compared to OUTB. N4 and N5 will be driven approximately the same and will split I_B equally, and thus no differential voltage will appear across OUT/OUTB as a result of amplifier 153. The net effect is a negative differential voltage between OUT and OUTB, indicating that Din should be set to a logic low condition.

Several features of this embodiment are evident. First, the two differential amplifiers nominally complement each other—when one receives a differential input voltage, the other does not, and therefore both can drive the same load circuit to create a common output. Second, the reference values all correspond to values generated on transmission line 80, which can therefore be generated fairly accurately. Third, the differential input voltage that is

nominally amplified is $0.5V_{DD}$, whereas the prior art single-amplifier configurations amplify a $0.25V_{DD}$ differential signal for the same voltage.

For low-voltage signaling, the embodiment of Figure 8 is particularly useful because it uses larger differential input voltages and therefore has a superior noise margin. For instance, consider a case where V_{DD} = 1 V and V_{SS} = 0 V and two drivers are both trying to drive V_{BL} to V_{DD}, but because of noise or other effects V_{BL} = 0.8 V. A prior art receiver would compare V_{BL} = 0.8 V to $VREFH$ = 0.75 V and attempt to sense a logic high signal from a 0.05 V differential voltage. Receiver 150, on the other hand, would amplify a 0.3 V differential signal in differential amplifier 151, and an opposing -0.2 V differential signal in differential amplifier 153, which is equivalent to amplifying a 0.1 V differential voltage in a prior art receiver. Thus receiver 150 has twice the noise margin of a prior art receiver.

Figure 9 illustrates one embodiment for reference selector 130 of Figure 4. A low voltage VL is applied to the source of a P-channel MOSFET transistor P7, and a high voltage VH is applied to the source of an N-channel MOSFET transistor N7. The drains of transistors P7 and N7 are both connected to supply VREFD1, the output of reference selector 130. The gates of transistors P7 and N7 are both connected to DOUT1. When DOUT1 is a logic high signal, VH is passed as VREFD1, and when DOUT1 is a logic low signal, VL is passed as VREFD1. VL and VH may be adjusted if necessary to account for the threshold voltages of P7 and N7 such that VREFD1 approximate high and low voltages.

Figure 10 illustrates a second embodiment for reference selector 130 of Figure 4. Two transmission gates T1 and T2 are both connected to VREFD1, the output of reference selector 130. A low voltage VL is connected to the input of T1, and a high voltage VH is connected to the input of T2. DOUT1 is connected to the input of an inverter I1, which generates the logical inverse of DOUT1, DOUT1#. DOUT1 and DOUT1# are applied to the control gates of transmission gate T1 such that T1 is on when DOUT1 is logic low. DOUT1

and DOUT1# are applied to the opposite control gate terminals of transmission gate T2 such that T2 is on when DOUT1 is logic high.

Figure 11 illustrates a circuit diagram for one embodiment of receiver 350 of Figure 6, which accepts four reference voltages V_{DD}, V_{SS}, VREFM1, and VREFM2. Instead of the Figure 4/Figure 7 approach of multiplexing two reference voltages to the same transistor gate (transistor N5), each reference voltage in Figure 11 is supplied to the gate of its own transistor in its own differential amplifier. Different differential amplifiers are activated and deactivated depending on the state of Dout1.

Receiver 350 contains a load circuit 355 and differential amplifiers 351 like the corresponding circuits in receiver 150. In receiver 350, however, VREFM1 is applied to the gate of N1 and V_{DD} is applied to the gate of N5, since these are the two comparison voltages to be used when Dout1 is a logic high value.

A control voltage BIAS1 is applied to tail current transistors N3 and N6, causing them to generate matching tail currents I_{A1} and I_{B1}, respectively. BIAS1 can be shorted to ground through a transistor N14, however, causing transistors N3 and N6 to turn off. The logic signal Dout1 is applied to the input of an inverter I2 to produce the logical inverse of Dout1, Dout1#. Dout1# is applied to the gate of transistor N14, such that N14 remains off when Dout1 is in a logic high state (time periods T1 and T2 of Figure 7A), causing differential amplifiers 351 and 353 to perform comparisons as previously described for amplifiers 151 and 153 of Figure 8. When Dout1 is in a logic low state, however, (time periods T3 and T4 of Figure 7A), Dout1# activates N14 to turn off current flow through differential amplifiers 351 and 353.

Receiver 350 includes a duplicate set of differential amplifiers 357 and 359, which are activated when differential amplifiers 351 and 353 are deactivated, and vice versa. Differential amplifier 357 contains a matched differential transistor pair N8 and N9 and a

current source transistor N10. Transistor N8 receives a gate voltage VREFM2. Transistor N9 receives a gate voltage V_{BL}. Preferably, transistors N8 and N9 are matched to transistors N1 and N2 as well, although this is not strictly necessary.

Differential amplifier 359 contains a matched differential transistor pair N11 and N12 and a current source transistor N13. Transistor N11 receives a gate voltage V_{BL}. Transistor N12 receives a gate voltage V_{SS}. Preferably, transistors N11 and N12 are matched to transistors N4 and N5 as well, although this is not strictly necessary.

A control voltage BIAS2 is applied to tail current transistors N10 and N13, causing them to generate matching tail currents I_{A2} and I_{B2}, respectively. Preferably, BIAS1 = BIAS2 and N10, N13 are matched to N3, N6, such that I_{A2} and I_{B2} have the same magnitude as I_{A1} and I_{B1} when activated. BIAS2 can be shorted to ground through a transistor N15, causing transistors N10 and N13 to turn off. Dout1 is applied to the gate of transistor N15, such that N15 remains off when Dout1 is in a logic low state (time periods T3 and T4 of Figure 7A), causing differential amplifiers 357 and 359 to perform comparisons as previously described for amplifiers 151 and 153 of Figure 8. When Dout1 is in a logic high state, however, (time periods T1 and T2 of Figure 7A), Dout1 activates N15 to turn off current flow through differential amplifiers 357 and 359.

BIAS1 and BIAS2 can be supplied from individual bias circuits. In the alternative, BIAS1 and BIAS2 can be supplied from a common BIAS circuit that connects to BIAS1 and BIAS2 through pass transistors (not shown) that disconnect BIAS1 or BIAS2 from BIAS when BIAS1 or BIAS2 will be shorted to ground.

Inverter-type drivers can be used in each of the described embodiments. Figure 12 shows a circuit diagram for an alternate embodiment of driver 110. Driver 110 connects a resistor 112 between V_{DD} and output node 120. Output node 120 is also connected to V_{SS} through a serial combination of two n-channel transistors N20 and N21. N20 receives a gate

voltage VGATE, e.g., fixed at $V_{DD}/2$. N21 receives as its gate voltage the output of an inverter I3, which has its input connected to Dout1. When Dout1 is at a logic high value, transistor N21 is turned off and node 120 is pulled up through resistor 112. When Dout1 is at a logic low value, transistor N21 is turned on and node 120 is also pulled down through transistors N20 and N21. Driver 110 has a small input capacitance as compared to an inverter-type driver.

Those skilled in the art will recognize that many other device configuration permutations can be envisioned and many design parameters have not been discussed. For example, the circuit of Figure 11 could be adapted to a three-reference voltage system with only one midpoint voltage by using three differential amplifiers and having the one receiving the midpoint voltage unswitched. Or, reference selector 130 of Figure 4 could be adapted to multiplex two midpoint voltages, allowing the receiver of Figure 8 to be used in the system of Figure 6. Specific voltages, resistance values, transistor sizes, etc., have not been specified as these will change from application to application. Likewise, functionality shown embodied in a single functional block may be implemented using multiple cooperating circuits or blocks, or vice versa. The integrated circuits described can be any type of circuit that inputs digital data from and sends digital data to another circuit, e.g., a microprocessor or other programmable processor, a memory controller, a memory device, a serializer/deserializer, etc. Such minor modifications and implementation details are encompassed within the embodiments of the invention, and are intended to fall within the scope of the claims.

The preceding embodiments are exemplary. Although the specification may refer to "an", "one", "another", or "some" embodiment(s) in several locations, this does not necessarily mean that each such reference is to the same embodiment(s), or that the feature only applies to a single embodiment.